Notice of Allowability	Application No.	Applicant(s)	
	10/034,717	LITT, TIMOTHE	
	Examiner	Art Unit	
	Tim Bonura	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the appeal brief filed 11/01/2005*.

2. ☒ The allowed claim(s) is/are *1,6-18,20-23,25 and 27-29*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *01/03/2006* .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Allen Christenson on 01/03/2006.

3. The application has been amended as follows:

a. Regarding claim **1**, **amend claim** to read as follows:

i. An integrated circuit fabricated on a chip, comprising: an on-chip logic analyzer a cache memory that includes a plurality of cache sets; at least one on-chip logic device that stores data to said plurality of cache sets during normal operation; and a logic gate that receives an enable signal when the on-chip logic analyzer is enabled, and which disables at least one of said plurality of said cache set for storing data from said on-chip logic analyzer; wherein the integrated circuit comprises a processor, and the on-chip logic device includes a CPU core; wherein the enable signal is generated by the on-chip logic analyzer; wherein the logic comprises a multiplexer that connects the on-chip logic analyzer to the disabled cache set when the on-chip logic analyzer asserts the enable signal; wherein the multiplexer forms part of a cache controller.

b. Regarding claims **2-5**, **cancel claims**.

c. Regarding claims **6-11**, claims are to remain **previously presented**.

d. Regarding claim **12**, **amend claim** to read as follows:

ii. A processor comprising: a CPU core; a cache memory coupled to said CPU core; said cache memory including a plurality of cache sets that during normal operation store data written by the CPU core; and at least one logic analyzer that receives information relating to the internal state of the processor, said logic analyzer being coupled to at least one of said plurality of cache set; and wherein said logic analyzer is capable of gaining ownership of said at least one cache set to store selected portions of said received information when said on-chip logic analyzer is enabled; wherein data stored by the logic analyzer is assigned an address range, and said at least one cache set makes available at least a portion of the data stored therein when a read request is made to the address range assigned to the logic analyzer.

e. Regarding claims **13-18**, claims are to remain **previously presented**.

f. Regarding claim **19**, **cancel claim**.

g. Regarding claim **20, amend claim** to read as follows:

iii. The processor of claim ~~19~~ 8, wherein the logic analyzer includes an addressable read register that receives data stored in the at least one cache set in response to a read request to an address range assigned to the on-chip logic analyzer.

h. Regarding claim **21**, **amend claim** to read as follows:

iv. A processor fabricated on a chip comprising: a cache memory divided into a plurality of cache sets; test logic coupled to said cache memory, which tests the cache sets during system initialization and determines which cache sets are operative; a cache controller that controls the storage and retrieval of data from said cache memory, with said cache controller only storing data to cache

sets that are determined to be operative by the test logic; a CPU core coupled to said cache memory, said CPU core storing data to all operative cache sets during normal operation; an on-chip logic analyzer capable of receiving data reflecting the internal state of the processor, said on-chip logic analyzer coupled to at least one cache set, which is disabled from use by the CPU core when the on-chip logic analyzer is enabled; wherein the on-chip logic analyzer is capable of issuing a read request to the cache controller for data stored in the disabled cache set, which includes a signal indicating that the cache controller should force a hit on the disabled cache set.

i. Regarding claims **22-23**, claims are to remain **previously presented**.

j. Regarding claim **24**, **cancel claim**.

k. Regarding claim **25**, **amend claim** to read as follows:

v. A method of maintaining state data of a processor in a cache memory set, comprising the acts of: enabling an on-chip logic analyzer to receive and select data for storage; disabling a cache set from use by any device other than the on-chip analyzer; storing said selected data in the disabled cache set; further comprising the acts of: reading said selected data from said disabled cache set; and storing said data read from the disabled cache set to an addressable register.

l. Regarding claim **26**, **cancel claim.**

m. Regarding claim **27**, claim is to remain **previously presented**.

n. Regarding claim **28**, **amend claim** to read as follows:

vi. The method of claim ~~26~~ 19, wherein the act of reading selected data includes: issuing a read request to an 1/0 address reserved for on-chip logic

analyzer data; recognizing the read request as targeting on-chip logic analyzer data; routing the read request to the cache memory; and forcing a hit on the disabled cache set.

o. Regarding claim **29**, claim is to remain **previously presented**.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Tim Bonura.**

- The examiner can normally be reached on **Mon-Fri: 8:30-5:00**.
- The examiner can be reached at: **571-272-3654**.

5. If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, **Scott Baderman.**

- The supervisor can be reached on **571-272-3644.**

6. The fax phone numbers for the organization where this application or proceeding is assigned are:

- **703-872-9306 for all patent related correspondence by FAX.**

7. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov/. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

8. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **receptionist** whose telephone number is: **571-272-2100.**

9. Responses should be mailed to:

- **Commissioner of Patents and Trademarks**

  P.O. Box 1450

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tmb
January 3, 2006

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER